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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,402	07/21/2006	Hui Wang	495152002400	3574

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EXAMINER
RIPA, BRYAN D

ART UNIT	PAPER NUMBER
1723	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,402	WANG ET AL.	
	Examiner	Art Unit	
	BRYAN D. RIPA	1795	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 June 2005 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 9/6/06.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (W.I.P.O. Pub. No. 99/41434A2) (hereinafter referred to as "WANG") in view of Mizutani (U.S. Pat. No. 5,721,605) (hereinafter referred to as "MIZUTANI") with evidence from Pasciak (U.S. Pat. No. 4,808,000) (hereinafter referred to as "PASCIAK") and Batz et al., (W.I.P.O. Pub. No. 99/17344A1) (hereinafter referred to as "BATZ").

Regarding claim 1, WANG teaches an apparatus for electropolishing and/or electroplating metal layers on a semiconductor wafer the apparatus comprising:

- a receptacle having a plurality of section walls (see figure 3b below showing a cup-type receptacle having a plurality of section walls; see also page 27 line 26-page 28 line 16); and
- a wafer chuck configured to hold the semiconductor wafer and to position the semiconductor wafer within the receptacle with a surface of the semiconductor wafer adjacent to top portions of the plurality of section walls (see 29 below).

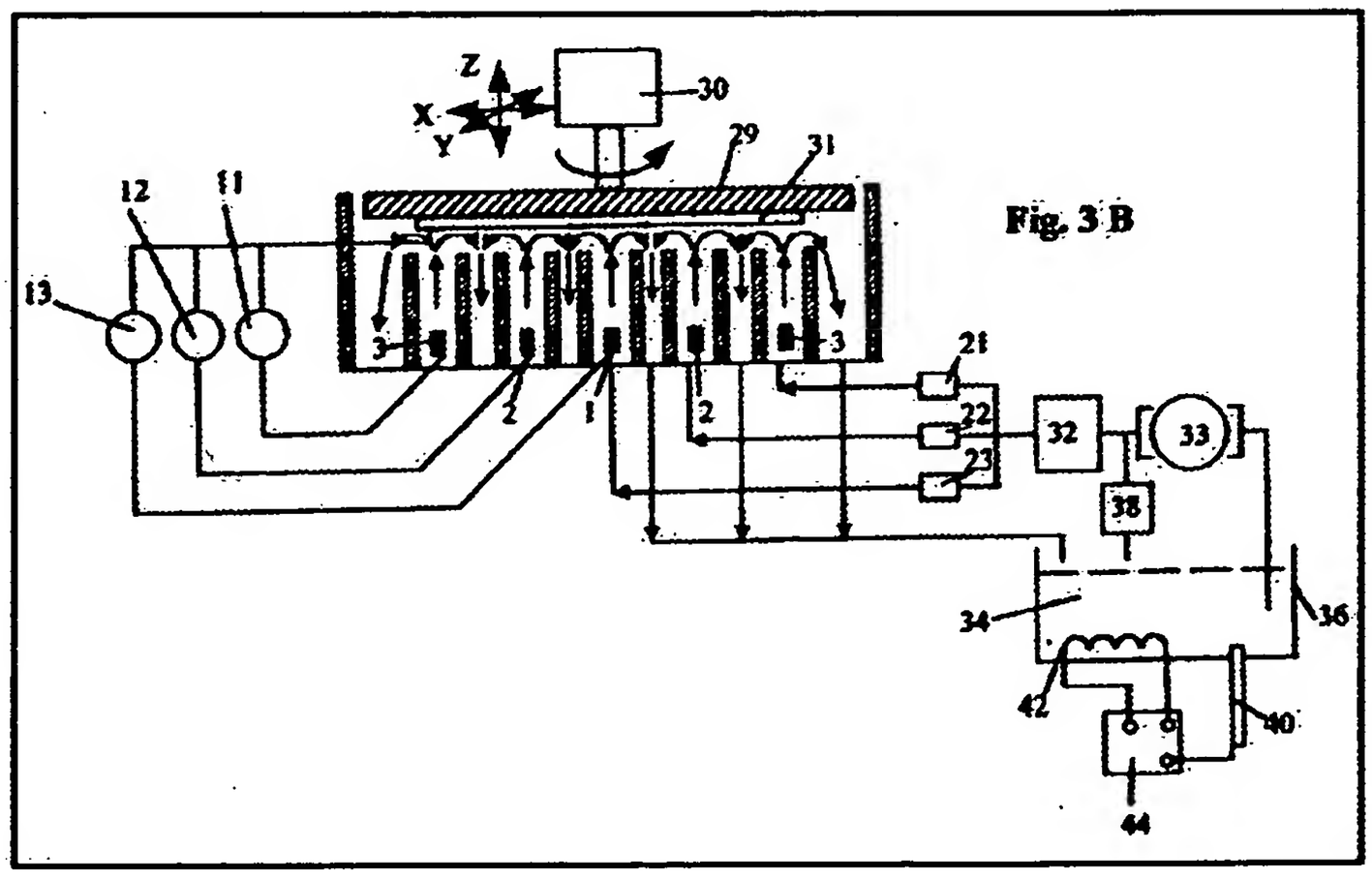
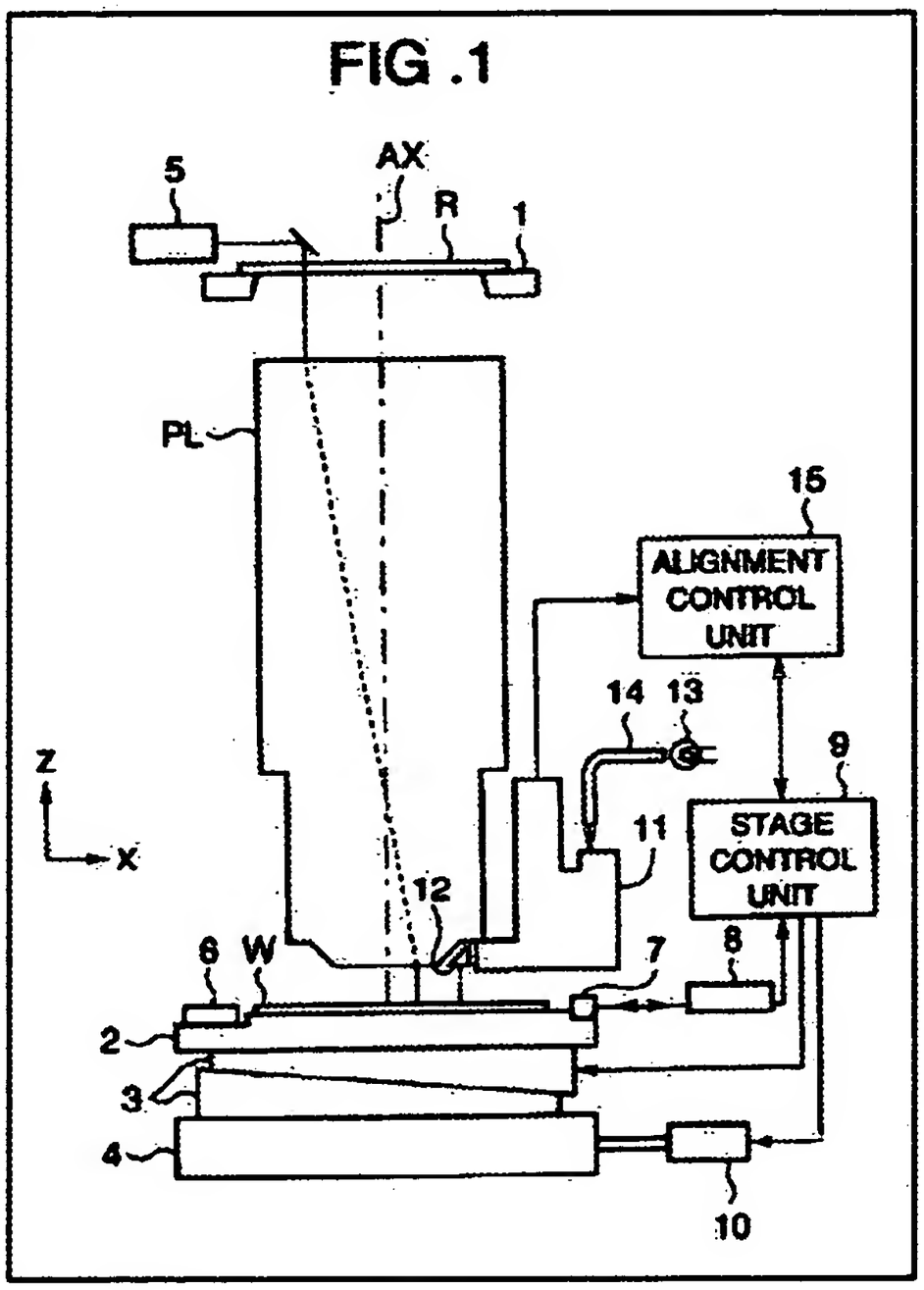


Fig. 3 B

WANG fails to explicitly teach there being a plurality of sensors configured to measure alignment between a center of one of the plurality of section walls and a center of the wafer chuck.

MIZUTANI, however, teaches the use of sensors to measure alignment of a wafer holder having a wafer disposed within it and an exposure apparatus (see laser interferometer 8 in figure 1 below; see also col. 3 lines 51-58).

FIG .1



Additionally, as evidenced by PASCIAK, the use of sensors for measuring the alignment and positioning of desired components is known in the art (see figures 1 and 2 and col. 2 lines 24-49; col. 3 line 9-col. 4 line 19 teaching generally the idea of using light sensors to align a tool and the workpiece so as to position the tool at an exact

location). Also, as evidenced by BATZ, the use of a position sensor to provide position information regarding the position of a wafer chuck in an electroplating apparatus is known in the art (see generally page 6; see also page 8 lines 9-15 teaching the electroplating apparatus having a sensor for detecting the vertical position of the wafer chuck in relation to the top of the receptacle containing the electrolyte solution).

Furthermore, although MIZUTANI teaches alignment of the wafer holder to an exposure apparatus, one of ordinary skill in the art would have readily appreciated that the sensors used to measure the alignment of the wafer holder could also be applied to other semiconductor processes in which alignment of the wafer with another object would be necessary. Additionally, MIZUTANI teaches the application of the aligning device in other applications besides the specific embodiment disclosed using an exposure apparatus (see col. 1 lines 8-14).

Moreover, based on the disclosure of WANG, one of ordinary skill in the art would have readily appreciated the need for accurate alignment between the receptacle and the wafer chuck since both the current and the flow of electrolyte by the plating system was specifically calculated based on the area of the substrate exposed to the particular area above the receptacle (see page 29 lines 16-23). It would have been readily obvious that any variation in the alignment could potentially result in the altering of the estimated area to be treated as well as causing the treatment of the substrate to occur in areas not contemplated originally due to the initial assumption of alignment of the wafer chuck and receptacle.

Consequently, in order to further improve quality assurance and control, one of ordinary skill in the art would have readily appreciated the benefit of having sensors like that employed by MIZUTANI, in the electroplating apparatus of WANG in order to facilitate improved alignment between the wafer chuck and the receptacle. Furthermore, one of ordinary skill in the art would also have been motivated to add alignment sensors, like that employed by MIZUTANI, to the apparatus of WANG in order to achieve better plating performance through the increased process control achievable by the improved alignment.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate a plurality of sensors configured to measure alignment as claimed in the electroplating apparatus of WANG.

Regarding claims 2 and 3, WANG as modified by MIZUTANI does not explicitly teach the tolerance being within the ranges as claimed. However, it would have been obvious to want to maximize the alignment to the greatest extent possible, i.e. minimize the tolerance. Consequently, it would have been readily obvious to one of ordinary skill in the art using the light sensors to minimize variances in the alignment of the workpiece and the receptacle to within the claimed ranges.

Regarding claim 4, WANG teaches the apparatus for electropolishing and/or electroplating metal layers on a semiconductor wafer wherein the plurality of section walls are cylindrical and concentric (see figure 3b above).

Regarding claims 5-13, WANG as modified by MIZUTANI does not explicitly teach the placement of the sensors as claimed. However, it would have been readily obvious to one of ordinary skill in the art to place the sensors in proximity to each other in such a way so as to be able to effectively function to align the wafer chuck and the receptacle. As a result one of ordinary skill would have recognized the need to place the sensors on both the receptacle and the wafer chuck at the various locations to achieve that result.

Consequently, the limitations of claims 5-13 as to the location of the placement of the sensors would have been readily obvious to one of ordinary skill in the art given the working requirements of the sensors and their intended purpose.

Regarding claim 14, WANG as modified by MIZUTANI teaches the apparatus for electropolishing and/or electroplating metal layers on a semiconductor wafer wherein the first plurality of sensors includes optical reflectivity sensors (see MIZUTANI col. 3 lines 51-54 teaching the use of a laser interferometer as the position sensor; see also col. 1 lines 41-45 teaching the use of a laser step alignment sensor which measures alignment by reflectivity as claimed). Furthermore, it would have been obvious that other types of optical sensors, such as the laser step alignment sensor, could be used in order to provide the necessary alignment of the wafer chuck and receptacle in the electroplating apparatus of WANG.

Regarding claims 15 and 18, WANG as modified by MIZUTANI does not explicitly teach the sensors being used to configure the vertical position of the wafer check relative to the receptacle. However, as evidenced by BATZ, the use of a position sensor or monitoring means for detecting and sensing the vertical position of the wafer chuck in relation to the receptacle containing the electrolyte bath solution is known in the art (see BATZ at page 8 lines 9-15 teaching the electroplating apparatus having a sensor for detecting the vertical position of the wafer chuck in relation to the top of the receptacle containing the electrolyte solution).

Moreover, as in WANG, where the vertical position of the wafer chuck in relation to the receptacle is critical to know to ensure proper contact with the plating solution one of ordinary skill in the art would have readily appreciated the benefit of having sensors disposed within the apparatus for this function. Furthermore, one of ordinary skill in the art would have been motivated to include sensors for determining the vertical position since it would enable the device to be used for some of the more complicated plating protocols wherein in order to achieve a more uniform plating profile only a certain portion of the wafer is plated in order to compensate for variations in the normal plating process.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include a second plurality of sensors configured to measure the vertical gap between the wafer chuck and the receptacle as claimed.

Regarding claims 16 and 17, WANG fails to explicitly teach the apparatus for electropolishing and/or electroplating metal layers on a semiconductor wafer wherein the gap between the semiconductor wafer and the top portion of the plurality of section walls is between a range of 0.5 millimeters to 10 millimeters and further 5 millimeters. However, WANG does teach an embodiment where the gap between the wafer and the anode is around 5 mm (see page 45 lines 1-2 teaching the gap being between 0.1 mm and 5 mm).

Furthermore, it would have been within the capability of one having ordinary skill in the art through routine experiment to come to an optimum distance between the top of the receptacle and the semiconductor wafer so as to provide for a complete coverage of the wafer with electrolyte while still providing sufficient room for the electrolyte to evenly flow towards the outer cylindrical walls without generating excessive turbulent flow which could act to create localized areas of high and low plating.

Regarding claim 19, see the discussion above with respect to claim 14.

Regarding claims 20 and 21, see the discussion above with respect to the rejection of claim 1.

Regarding claims 22, 25 and 26, see the discussion above with respect to the rejection of claims 5-13.

Regarding claims 23 and 27, see the discussion above with respect to the rejection of claim 1. Additionally, it would have been readily obvious that in order to provide for the proper alignment of the wafer chuck in relation to the position of the receptacle that there would need to be a pair of sensors positioned 90 degrees from each other in order to provide for alignment along the x and y planes using the axis as set forth in figure 3b of WANG. As a result, for at least the reasons as listed previously with respect to the rejection of claim 1, it would also have been further obvious to provide for sensor pairs as claimed.

Regarding claim 28, WANG as modified by MIZUTANI teaches a method of electropolishing and/or electroplating metal layers on a semiconductor wafer, the method comprising:

- positioning a wafer chuck holding a semiconductor wafer within a receptacle having a plurality of section walls, wherein a surface of the semiconductor wafer to be electropolished or electroplated is positioned adjacent to top portions of the plurality of section walls (see wafer chuck 29 and figure 3b above showing a cup-type receptacle having a plurality of section walls; see also page 27 line 26-page 28 line 16).

WANG fails to teach measuring alignment between a center of one of the plurality of section walls to a center of the wafer chuck using a first plurality of sensors.

MIZUTANI, however, teaches the use of sensors to measure alignment of a wafer holder having a wafer disposed within it and an exposure apparatus (see laser interferometer 8 in figure 1 above; see also col. 3 lines 51-58).

Additionally, as evidenced by PASCIAK, the use of sensors for measuring the alignment and positioning of desired components is known in the art (see figures 1 and 2 and col. 2 lines 24-49; col. 3 line 9-col. 4 line 19 teaching generally the idea of using light sensors to align a tool and the workpiece so as to position the tool at an exact location). Also, as evidenced by BATZ, the use of a position sensor to provide position information regarding the position of a wafer chuck in an electroplating apparatus is known in the art (see generally page 6; see also page 8 lines 9-15 teaching the electroplating apparatus having a sensor for detecting the vertical position of the wafer chuck in relation to the top of the receptacle containing the electrolyte solution).

Furthermore, although MIZUTANI teaches alignment of the wafer holder to an exposure apparatus, one of ordinary skill in the art would have readily appreciated that the sensors used to measure the alignment of the wafer holder could also be applied to other semiconductor processes in which alignment of the wafer with another object would be necessary. Additionally, MIZUTANI teaches the application of the aligning device in other applications besides the specific embodiment disclosed using an exposure apparatus (see col. 1 lines 8-14).

Moreover, based on the disclosure of WANG, one of ordinary skill in the art would have readily appreciated the need of accurate alignment between the receptacle and the wafer chuck since the both the current and the flow of electrolyte by the plating

system was specifically calculated based on the area of the substrate exposed to the particular area above the receptacle (see page 29 lines 16-23). It would have been readily obvious that any variation in the alignment could potentially result in the altering of the estimated area to be treated as well as causing the treatment of the substrate to occur in areas not contemplated originally due to the initial assumption of alignment of the wafer chuck and receptacle.

Consequently, in order to further improve quality assurance and control, one of ordinary skill in the art would have readily appreciated the benefit in having sensors like that employed by MIZUTANI, in the electroplating method of WANG in order to facilitate improved alignment between the wafer chuck and the receptacle. Furthermore, one of ordinary skill in the art would also have been motivated to add alignment sensors, like that employed by MIZUTANI, for use in the method of WANG in order to achieve better plating performance through the increased process control achievable by the improved alignment.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate a plurality of sensors configured to measure alignment of the electroplating apparatus of WANG for use in the electroplating method as claimed.

Regarding claims 29-33, see the discussion above with respect to the rejection of claims 5-13 as to the placement of the sensor pairs. Furthermore, with respect to the limitations regarding the measuring steps, it is implicit in the prior art teachings

regarding the aligning of two objects that one would measure the space or gap at two points within the area to be aligned and then adjust the alignment according to the two measurements. As such, it would have been obvious to one of ordinary skill in the art at the time of invention to have two measuring steps followed by an alignment step as claimed for each of the various configurations.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1) Van Der Muehlen et al., (U.S. Pat. No. 6,489,626) (hereinafter referred to as "MUEHLEN") teaching the use of a light sensor for detecting the position of a wafer (see col. 4 lines 20-46).

2) Volovich (U.S. Pat. No. 5,238,354) (hereinafter referred to as "VOLOVICH") teaching the use of a light sensor for detecting the position of a wafer (see col. 3 lines 35-44).

3) Zheng et al., (U.S. Pat. No. 6,911,136) (hereinafter referred to as "ZHENG") teaching the use of a sensor to detect the position of a wafer in an electroplating process (see col. 4 lines 15-21).

4) Hunter (U.S. Pat. No. 6,244,121) (hereinafter referred to as "HUNTER") teaching the use of a laser to detect alignment of a wafer by measuring the distance at various points (see col. 3 line 58-col. 4 line 6).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRYAN D. RIPA whose telephone number is 571-270-7875. The examiner can normally be reached on Monday to Friday, 9:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexa Neckel can be reached on 571-272-1446. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Harry D Wilkins, III/
Primary Examiner, Art Unit 1795

/B. D. R./
Examiner, Art Unit 1795